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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/694,411
Filing Date: October 23, 2000
Appellant(s): GARDINER ET AL.

Steve M. Perry
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/27/2007 appealing from the Office action mailed 2/27/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is deficient. 37 CFR 41.37(c)(1)(v) requires the summary of claimed subject matter to include: (1) a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number, and to the drawing, if any, by reference characters and (2) for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function as permitted by 35 U.S.C. 112, sixth paragraph, must be identified and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters.
The brief is deficient because: claim 10, step (c) should reference page 11, lines 5-11 not page 10 and the status of claim 10 is incorrect and should read as (currently amended).

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. Independent claim 32 is listed as both independent and dependent in part c.

(7) Claims Appendix

A substantially correct copy of appealed claims 10, 24 and 32 appears on pages 38-40 of the Appendix to the appellant's brief. The minor errors are as follows: The status of the claims is incorrect and should read as (currently amended) not (previously presented).

(8) Evidence Relied Upon

5864342	Kajiya et al.	1-1999
6853381	Grigor et al.	2-2005
6316974	Taraci et al.	11-2001

(9) Grounds of Rejection

Appellant is correct that the 102(e) rejection under Kajiya et al. should have been a 102(b) rejection and that the analysis of the rejection is unchanged since the rejection, now based on 102(b), is the same. Examiner has corrected this oversight.

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10, 11 and 13 rejected under 35 U.S.C. 102(b) as being anticipated by Kajiya et al. U.S. Patent No. 5864342.

Referring to claim 10, Kajiya et al. teaches a method for enabling a single pixel frame buffer (column 6, lines 15-29, i.e. a single rasterization buffer is understood to be a single pixel frame buffer) for simultaneous rendering and display in a computer image generator comprising the steps of a) dividing a geometry buffer into a plurality of screen bins (column 10, lines 35-42, i.e. the scene/image is divided into pixel regions called chunks and the geometry is pre-sorted into bins based on which chunk the geometry will be rendered into); (b) storing primitives in each screen bin the primitives touch (column 10, lines 40-44; columns 15-16, lines 59-2, i.e. the geometry is pre-sorted into bins based on which chunk the geometry will be rendered into and geometry that

overlaps a chunk boundary is referenced in each chunk it is visible in); (c) rendering the screen bins by row from top to bottom, into the single pixel frame buffer (column 6, lines 15-29; column 8, lines 45-51; column 16, lines 17-24; column 41, lines 20-27, i.e. the chunks are rendered from left-to-right, top-to-bottom scan order to a common depth buffer or rasterization buffer); and (d) displaying at least one row of screen bins rendered before the rendering of all the screen bins has completed, wherein the displaying of the screen bins takes place after a selected portion of the screen bins for a current field have been rendered (column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of displaying at least one row of screen bins is initiated after at least one row of screen bins/chunks has completed rendering and while a second row of screen bins/chunks is being rendered such that the selected portion of screen bins rendered prior to the initiation of the display step is understood to be one row/band of screen bins/chunks).

Referring to claim 11, the rationale for the rejection of claim 10 is incorporated herein, Kajiya et al. teaches a method as in claim 10, further comprising the step of reducing the transport delay without allowing the display step to overlap a rendering envelope (Fig. 22; column 56, lines 11-40).

Referring to claim 13, the rationale for the rejection of claim 10 is incorporated herein, Kajiya et al. teaches a method as in claim 10 further comprising the step of rendering at least one row of screen bins before the display step begins (column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of

displaying at least one row of screen bins is initiated after at least one row has completed rendering).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiya et al. in view of Grigor et al. U.S. Patent No. 6853381.

Referring to claim 12, the rationale for the rejection of claim 10 is incorporated herein, Kajiya et al. teaches a method as in claim 10 but does not specifically teach the step of reducing the transport delay and allowing the display step to overlap a rendering envelope.

Grigor et al. teaches this limitation (Abstract; Figs. 1 and 8; column 3, lines 13-33; column 8, lines 32-67, i.e. individual display lines comprising a plurality of pixels are rendered and stored in the frame buffer in a memory location only if the location has been previously accessed for display).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Kajiya et al. to include the teachings of Grigor et al. thereby overcoming the problems associated with single frame

buffers such as tearing, choppy video/graphics and stalling (columns 1-2, lines 32-13) by allowing the frame buffer to be utilized more efficiently (column 3, lines 46-50) and allowing for an efficient way to receive primitives to be displayed, while assuring the data integrity of the frame buffer (columns 9-10, lines 66-10).

Referring to claim 14, the rationale for the rejection of claim 10 is incorporated herein, Kajiya et al. teaches a method as in claim 10 further comprising but does not specifically teach the step of reducing the transport delay by allowing the display step to overlap a rendering envelope without allowing pixels from a previous field to be displayed.

Grigor et al. teaches this limitation (Abstract; Figs. 1 and 8; column 3, lines 13-33; column 5, lines 13-25 and 56-67; column 8, lines 32-67, i.e. individual display lines comprising a plurality of pixels are rendered and stored in the frame buffer in a memory location only if the location has been previously accessed for display and the PIXEL OFFSET and LINE INDICATOR are utilized to prevent the display of previously displayed pixels).

The rationale for combining Kajiya et al. with the teachings of Grigor et al. as found in the motivation statement of claim 12 is incorporated herein.

Claims 24, 26-29, 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiya et al. in view of Taraci et al. U.S. Patent No. 6316974.

Referring to claim 24, Kajiya et al. teaches a method for enabling a single pixel frame buffer (column 6, lines 15-29, i.e. a single rasterization buffer is understood to be

a single pixel frame buffer) for simultaneous rendering and display in a computer image generator comprising the steps of a) dividing a geometry buffer into a plurality of screen bins (column 10, lines 35-42, i.e. the scene/image is divided into pixel regions called chunks and the geometry is pre-sorted into bins based on which chunk the geometry will be rendered into); (b) storing primitives in each screen bin the primitives touch (column 10, lines 40-44; columns 15-16, lines 59-2, i.e. the geometry is pre-sorted into bins based on which chunk the geometry will be rendered into and geometry that overlaps a chunk boundary is referenced in each chunk it is visible in); (c) rendering the screen bins by row from top to bottom, into the single pixel frame buffer (column 6, lines 15-29; column 8, lines 45-51; column 16, lines 17-24; column 41, lines 20-27, i.e. the chunks are rendered from left-to-right, top-to-bottom scan order to a common depth buffer or rasterization buffer) but does not specifically teach (d) displaying at least one rendered screen bin when the rendering of the screen bins for the single pixel frame buffer is at least ½ completed.

Taraci et al. teaches this limitation (column 8, lines 30-45, i.e. the output/display vertical frame read pointer is placed at a point in reference to the input/render vertical write pointer to create a frame rate delay of ½ a frame indicating that rendering is at least ½ completed before displaying begins).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Kajiya et al. to include the teachings of Taraci et al. thereby providing a system capable of locking the output vertical frame sync pulses to the input vertical frame sync pulses where the read and

write pointers do not cross and where it does not produce an output frame made up of two different input frames (Taraci et al.: column 8, lines 25-34 and 46-66).

Referring to claim 32, the rationale for the rejection of claim 24 is incorporated herein, Kajiya et al., as modified above, teaches an image generator with a single pixel frame buffer enabled for simultaneous rendering and display comprising a geometry buffer, a rendering engine, and a display processor for performing the method of claim 24 (Figs. 1-4B and 9-14).

Referring to claim 34, the rationale for the rejection of claim 32 is incorporated herein, Kajiya et al., as modified above, teaches an image generator as in claim 32, further comprising a geometry engine configured to transform a database and the plurality of primitives used by the image generator (Figs. 1, 4A and 4B; column 15, lines 59-67).

Referring to claim 35, the rationale for the rejection of claim 32 is incorporated herein, Kajiya et al., as modified above, teaches an image generator as in claim 32, further comprising a real-time controller configured to receive real-time control information and compute the transformation matrices (column 17, lines 4-9; column 61, lines 5-13).

(10) Response to Argument

Appellant's arguments filed 8/27/2007 have been fully considered but they are not persuasive.

Appellant argues, with regards to claims 10-14, that Kajiya et al. does not teach rendering into the single pixel frame buffer as claimed and cites column 6, lines 15-34 as teaching wherein the rasterization buffer is double buffered and column 16, lines 15-25 as teaching wherein the tiler uses double buffering to resolve the chunks.

Appellant further argues that Kajiya does not disclose the use of a single buffer compositing buffer, single buffer rasterization buffer, or any type of single buffer used to reduce transport delay.

Examiner respectfully submits that Kajiya, column 6, lines 15-34 teaches two alternative implementations of the raterization buffer, the first implementation is a common single rasterization buffer and the second implementation is a double-buffered rasterization buffer. Column 16, lines 15-25 teaches wherein the tiler uses a single common buffer with a free list to represent free memory in the common buffer that is allocated as new fragment record are generated and added to when fragment records are resolved. It should be noted that applicant claims wherein the screen bins are rendered to a single pixel frame buffer but the display step does not specifically claim displaying from a single buffer, see independent claims 10, 24 and 32. As can be seen in column 6, lines 15-34 and column 16, lines 15-24, Kajiya provides to option of using either a single buffer or a double-buffered rasterization buffer as alternative

embodiments. Therefore Kajiya does teach wherein the geometry can be rendered to a common/single rasterization/frame buffer as claimed.

Appellant then argues that Kajiya et al. does not describe the added complexity that would be needed to enable two separate processes to read and write to the same memory to allow simultaneous rendering and display, as previously described, see page 30, 2nd paragraph.

In response to appellant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the added complexity that would be needed to enable two separate processes to read and write to the same memory to allow simultaneous rendering and display, page 30, 2nd paragraph) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant then argues, with respect to claims 24, 26-29, 32 and 34-35, that Taraci does not teach displaying at least one rendered screen bin when the rendering of the screen bins for the single pixel frame buffer is at least ½ completed.

Examiner respectfully submits that while primary reference Kajiya does teach displaying at least one row of rendered screen bins before the rendering of all the screen bins has been completed, see column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, Kajiya does not specifically teach wherein the processor begins to display the rendered screen bins when the rendering of all the screen bins is at least ½ completed, secondary reference Taraci et al. is depended upon to teach this

particular limitation, i.e. Taraci et al. teaches allowing the output read pointer to be placed at any point in reference to the input vertical pointer so that the frame rate delay could be adjusted to half a frame to ensure that the read and write pointers in memory do not cross, see column 8, lines 26-45, column 9, lines 8-18, column 10, lines 55-61, column 14, lines 62-67, i.e. once the input write pointer reaches half a frame then the output read pointer begins reading from the memory. Thus combining Kajiya with the teachings of Taraci et al. would allow for the use of a single frame buffer in order to reduce the amount of memory required while ensuring that previously rendered screen bins contained in the single pixel frame buffer that have not yet been read out to the display are not overwritten by newly rendered screen bins.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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